A1 Cont'd issued on February 23, 1999 as U.S. Patent No. 5,874,781; which is a continuation of application serial number 08/515,719, filed August 16, 1995 and now abandoned. --

On page 3, line 7, please change "5,232,060" to -- 5,323,060 --.

On page 5, line 3, please change "plain" to -- plane --.

On page 6, line 5, please replace the formula "$\alpha = \tan^{-1}\left(\frac{W}{L}\right)$" with -- $\alpha = 2\tan^{-1}\left(\frac{L}{W}\right)$ --.

On page 6, line 10, please replace the formula "$N = \frac{180}{\tan^{-1}\left(\frac{W}{L}\right)}$" with

-- $N = \frac{180}{2\tan^{-1}\left(\frac{L}{W}\right)}$ --.

On page 6, line 12, please replace "allowable separation distance, W, per unit length, L" with -- length, L, per allowable separation distance, W --.

A2

IN THE CLAIMS:

Please cancel claims 1-6 without prejudice.

Please add the following claims.

7. A method of stacking a plurality of die, comprising

mounting an upper die on a lower die; and

A3 Cont'd defining a minimum angular offset with said mounting, wherein said minimum angular offset allows access to a bonding site on said lower die.

8. The method in claim 7, further comprising a step of mounting a lowest die on a substrate.

B2 9. A method of manufacturing a multichip module including dies, comprising:

stacking all of said dies, wherein said stacking defines an offset angle with any two of

said dies; and

bonding wire to said dies.

10. The method in claim 9, wherein said step of stacking further comprises stacking all of said dies before said step of bonding wire to said dies.

11. The method in claim 9, wherein said step of bonding further comprises bonding all of said wire only after said step of stacking all of said dies.

12. A method of assembling a plurality of dies, comprising:

stacking said plurality of dies along an axis;

establishing an orientation for each die of said plurality of dies;

clearing a line of sight to contact areas of any immediately underlying die with said orientation of said each die, wherein said line of sight is parallel to said axis; and

clearing said line of sight to contact areas of any underlying die with said orientation of said each die.

A3 Cont'd

13. A method of stacking a plurality of chips

spiraling said plurality of chips around an axis perpendicular to said plurality of chips; and

ensuring bond pad clearance to each chip of said plurality of chips.

14. The method in claim 13, wherein said step of spiraling said plurality of chips around an axis further comprises spiraling said plurality of chips around an axis passing through said each chip.

15. The method in claim 14, wherein said step of spiraling said plurality of chips around an axis further comprises spiraling said plurality of chips around an axis passing through a center of said each chip.